

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Akira GODA, et al.

SERIAL NO: 09/556,777

GAU: 2822

FILED: April 25, 2000

EXAMINER: Ida M. SOWARD

FOR: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references cited in the attached Korean Office Action listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

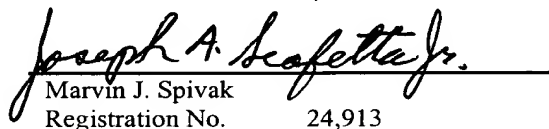
- ☒ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.


Marvin J. Spivak
Registration No. 24,913

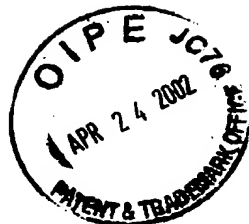
Joseph A. Scafetta, Jr.
Registration No. 26,803



22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/98)

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Mailed Date: March 27, 2002
Filing Due Date: May 27, 2002

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NOTIFICATION FOR FILING OPINION

Applicant: KABUSHIKI KAISHA TOSHIBA

Application No.: 10-2000-0022120

Title of Invention: Non-volatile Semiconductor Memory Device and Method for Manufacturing the Same

As the result of examination of the present application, the following reasons for rejection have been found and notified herein under Section 63 of the Patent Law. Any opinion about the rejection or any amendment must be filed by the above date. (The above date is extensible by one month for each request. No notification of allowing extension of time will be issued.)

[Reason]

The application fails to satisfy the requirements under Section 42 (3) of the Patent Law, on the grounds that the specification and the drawings are defective in the following respect.

The invention recited in claims 1-15 of the present application is unpatentable under Section 29 (2) of the Patent Law, as being such that the invention could easily have been made by a person with ordinary skill in the art to which the invention pertains, on the basis of the invention described in the following publications distributed in Japan or a foreign country prior to this application.

[Remarks]

1. In the identification number <78> of the detailed description, the term "element isolating region (12b)" is unclear, since it is inconsistent with the drawings (Section 42 (3)).

2. The invention of claims 1 to 15 are characterized by comprising an oxide film/a nitride film, which covers a gate electrode constituting a memory cell portion of a non-volatile memory element. Jpn. Pat. Appln. KOKAI Publication No. 11-074388 (disclosed March 16, 1999) shows a technology of forming an oxide film/a nitride film on a side wall of a

laminated gate and preventing the gate insulating film from thickening in the subsequent oxygen heat treatment. Jpn. Pat. Appln. KOKAI Publication No. 06-077497 (disclosed March 18, 1994) shows a technology of providing an antioxidation film of an oxide film/a nitride film formed so as to cover a laminated gate. Therefore, the present invention could have been easily achieved on the basis of the references (Section 29 (2)).

[Attachment]

Attachment 1: Jpn. Pat. Appln. KOKAI Publication No. 11-074388 (disclosed March 16, 1999)

Attachment 2: Jpn. Pat. Appln. KOKAI Publication No. 06-077497 (disclosed March 18, 1994)

March 27, 2002

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출력 일자: 2002/3/28

발송번호 : 9-5-2002-010074516

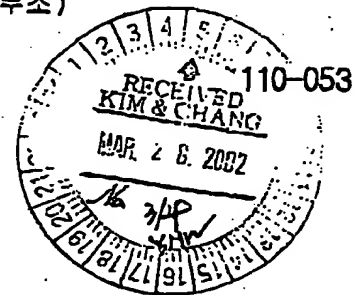
발송일자 : 2002.03.27

제출기일 : 2002.05.27

수신 : 서울 종로구 내자동 219 한누리빌딩(김&

장 특허법률사무소)

장수길 귀하



특허청 의견제출통지서

출원인

명칭 가부시끼가이샤 도시바 (출원인코드: 519980849672)

주소 일본국 도쿄도 미나토구 시바우라 1쵸메 1방 1고

대리인

성명 장수길 외 1명

주소 서울 종로구 내자동 219 한누리빌딩(김&장 특허법률사무소)

출원번호

10-2000-0022120

발명의 명칭

불휘발성 반도체 기억 장치 및 그 제조 방법

이 출원에 대한 심사결과 아래와 같은 거절이유가 있어 특허법 제63조의 규정에 의하여 이를 통지하오니 의견이 있거나 보정이 필요할 경우에는 상기 제출기일까지 의견서 또는/및 보정서를 제출하여 주시기 바랍니다. (상기 제출기일에 대하여 매회 1월 단위로 연장을 신청할 수 있으며, 이 신청에 대하여 별도의 기간연장승인통지는 하지 않습니다.)

[이유]

이 출원은 명세서 또는 도면의 기재가 아래에 지적한 바와 같이 불비하여 특허법 제42조제3항의 규정에 의한 요건을 충족하지 못하므로 특허를 받을 수 없습니다.
이 출원의 특허청구범위 제1항 내지 제15항에 기재된 발명은 그 출원전에 이 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 아래에 지적한 것에 의하여 용이하게 발명할 수 있는 것이므로 특허법 제29조제2항의 규정에 의하여 특허를 받을 수 없습니다.

[아래]

1. 상세한 설명의 식별번호 <7b>, "소자분리영역(12b)"의 기재는 도면과 일치하지 않고 불명료합니다. (제42조 제3항)

2. 청구항 제1항 내지 제15항은 불휘발성 메모리 소자의 메모리 셀부를 구성하는 게이트 전극을 피복하는 산화막/질화막을 갖는 것에 특징이 있는 것으로, 이는 일본특개평11-074388(공개일99.3.16)에는 적층 게이트의 측벽에 산화막/질화막을 형성하여 후속 산소 열처리시 게이트 절연막이 두꺼워지는 것을 방지하는 기술이 나타나 있고 일본특개평06-077497(공개일94.3.18)에는 적층 게이트를 덮도록 형성된 산화막/질화막의 산화방지막을 구비하는 기술이 나타나 있으므로 이들 인용예로부터 용이하게 발명할 수 있는 것에 해당됩니다. (제29조 제2항)

[참 부]

첨부 1 일본특개평11-074388(공개일99.3.16)

첨부2 일본특개평06-077497(공개일94.3.18) 끝.

출력 일자: 2002/3/28

2002.03.27

특허청

심사4국

반도체2 심사담당관실

심사관 오세준 

<<안내>>

문의사항이 있으시면 ☎ 042-481-5752 로 문의하시기 바랍니다.

특허청 직원 모두는 깨끗한 특허행정의 구현을 위하여 최선을 다하고 있습니다. 만약 업무처리과정에서 직원의 부조리행위가 있으면 신고하여 주시기 바랍니다.

▶ 홈페이지(www.kipo.go.kr)내 부조리신고센터